BT231V-800ET

4Q Triac

Rev.01 - 25 August 2025 Product data sheet

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT223-2L surface-mountable plastic package intended for applications requiring direct interfacing to logic level ICs and low power gate drivers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

4. Quick reference data

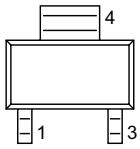
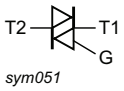
Table 1. Quick reference data

Symbol	Parameter	Conditions	Notes	Values			Unit
Absolute maximum rating							
V_{DRM}	repetitive peak off-state voltage			800			V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 117$ °C; Fig. 1; Fig. 2; Fig. 3		1			A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		11			A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		12.1			A
T_j	operating junction temperature			-40 to 150			°C
Symbol	**Parameter**	**Conditions**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 0.1$ A; T2+ G+; $T_j = 25$ °C; Fig. 7		-	-	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2+ G-; $T_j = 25$ °C; Fig. 7		-	-	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2- G-; $T_j = 25$ °C; Fig. 7		-	-	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2- G+; $T_j = 25$ °C; Fig. 7		-	-	25	mA

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	-	20	mA
V_T	on-state voltage	I_T = 1 A; T_j = 25 °C; Fig. 10		-	1.3	1.5	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		150	-	-	V/µs
dV_{com}/dt	rate of change of commutating voltage	V_D = 400 V; T_j = 125 °C; dI_{com}/dt = 0.5 A/ms; gate open circuit		0.5	-	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
3	G	gate		
4	T2	main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BT231V-800ET	SOT223-2L	BT231V-800ETF	Reel	4000	SOT223d-2L	02-Apr-2025

7. Marking

Table 4. Marking codes

Type number	Marking codes
BT231V-800ET	231V8E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DRM}	repetitive peak off-state voltage			800	V
V_{RRM}	repetitive peak reverse voltage			800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 117$ °C; Fig 1; Fig 2; Fig 3		1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig 4; Fig 5		11	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		12.1	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		0.61	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 20$ mA		50	A/µs
I_{GM}	peak gate current			1	A
P_{GM}	peak gate power			2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		0.1	W
T_{stg}	storage temperature			-40 to 150	°C
T_j	operating junction temperature			-40 to 150	°C

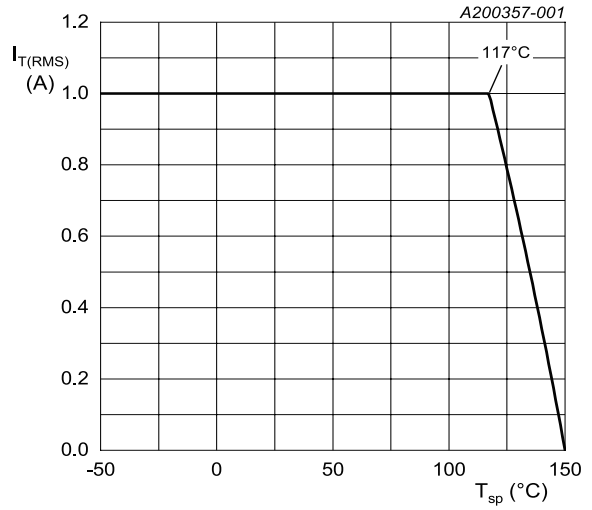
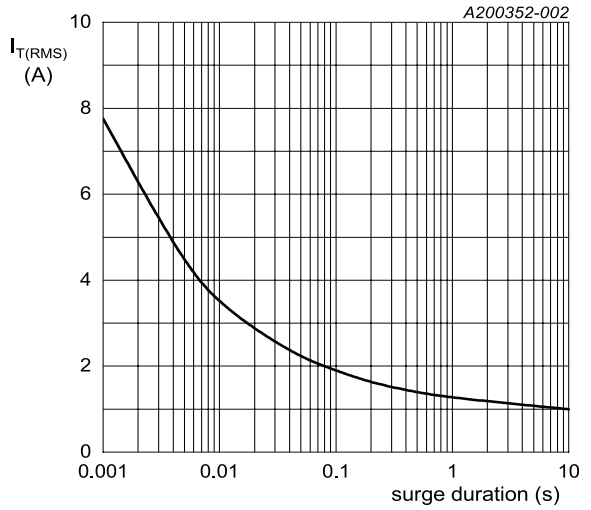
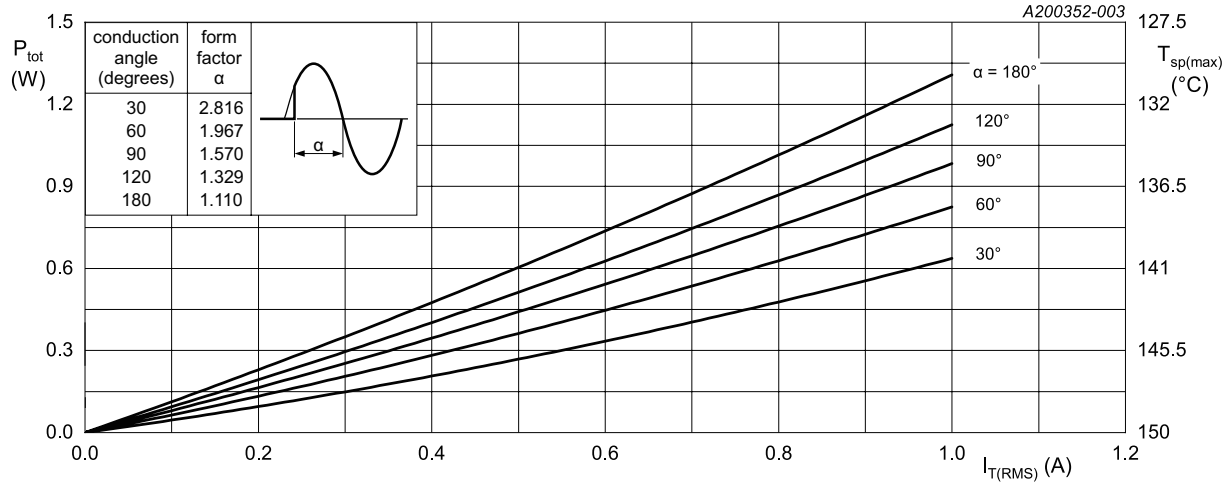


Fig. 1. RMS on-state current as a function of solder point temperature; maximum values



f = 50 Hz; T_{sp} = 117 °C

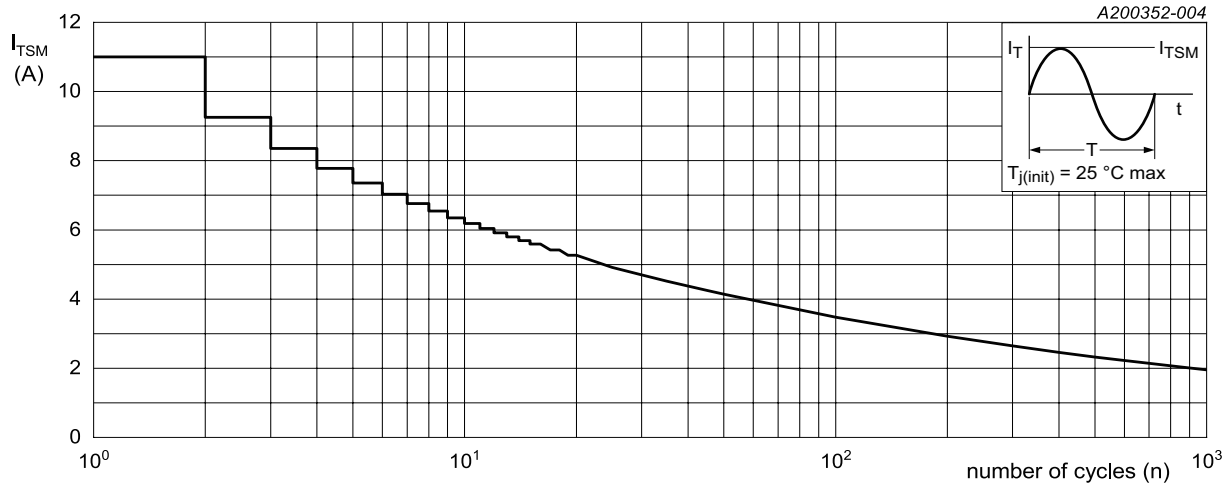
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

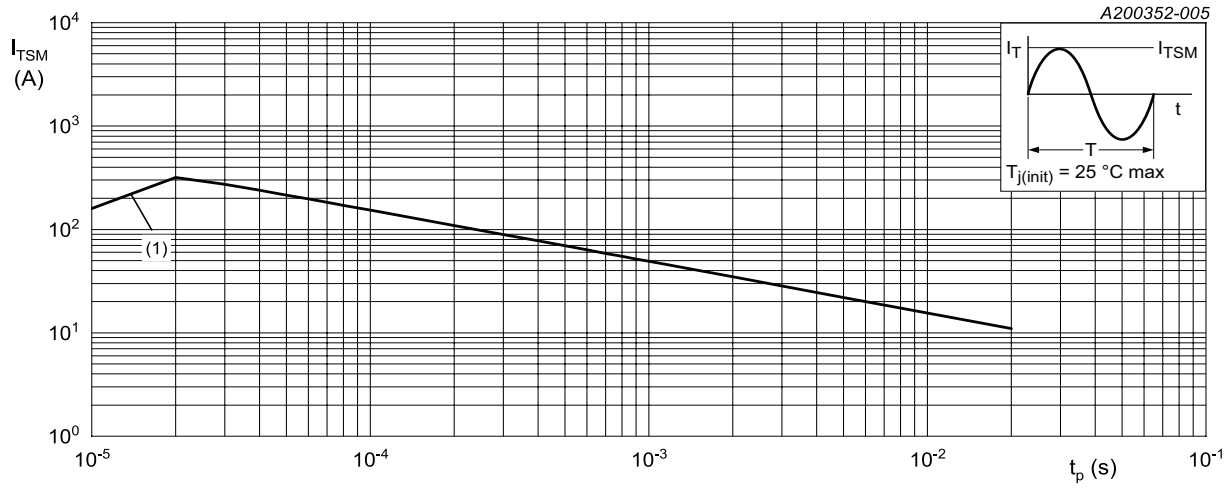
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



t_p ≤ 20 ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	full cycle; Fig 6		-	-	25	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; printed-circuit board mounted; pad area		-	65	-	K/W

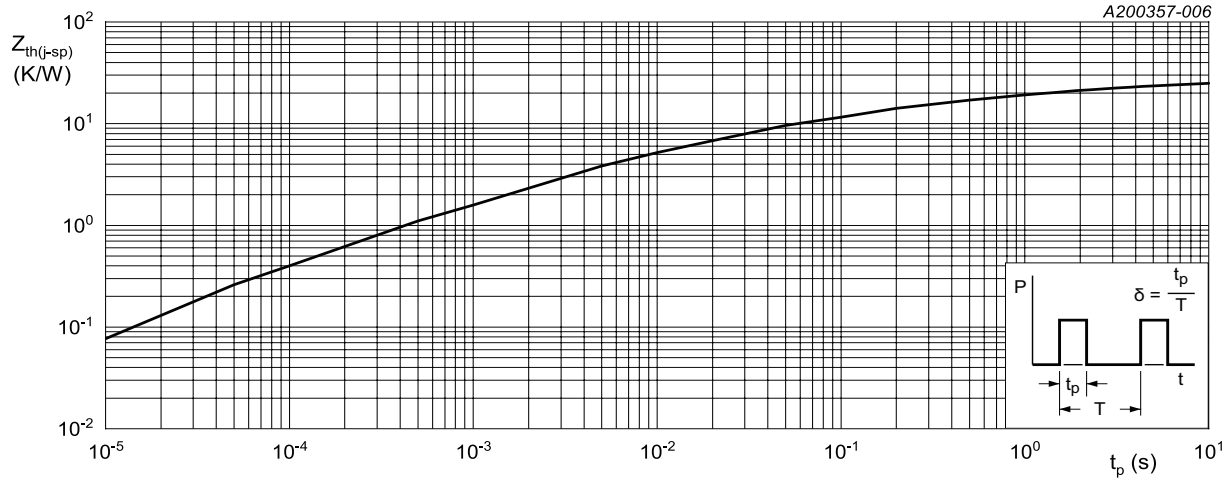
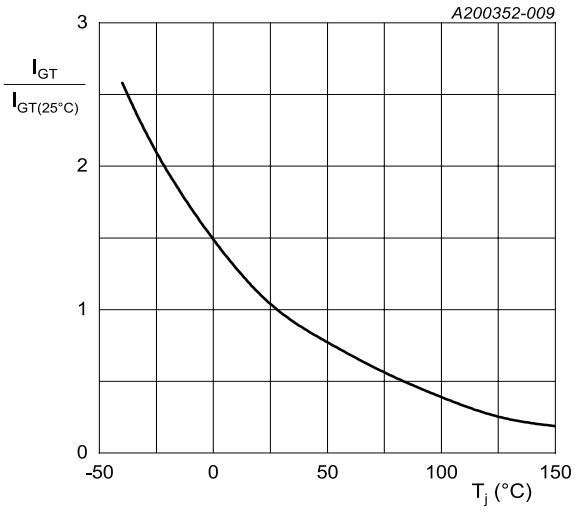


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		-	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		-	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		-	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2- G+; T_j = 25 °C; Fig. 7		-	-	25	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 8		-	-	15	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 8		-	-	15	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 8		-	-	15	mA
		V_D = 12 V; I_G = 0.1 A; T2- G+; T_j = 25 °C; Fig. 8		-	-	25	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	-	20	mA
V_T	on-state voltage	I_T = 1 A; T_j = 25 °C; Fig. 10		-	1.3	1.5	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	-	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 150 °C		0.2	-	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 150 °C		-	-	1	mA
I_R	reverse current	V_R = 800 V; T_j = 25 °C		-	-	10	µA
		V_R = 800 V; T_j = 150 °C		-	-	1	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		150	-	-	V/µs
dV_{com}/dt	rate of change of commutating voltage	V_D = 400 V; T_j = 125 °C; dI_{com}/dt = 0.5 A/ms; gate open circuit		0.5	-	-	V/µs



(1) T2- G+
(2) T2- G-
(3) T2+ G-
(4) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

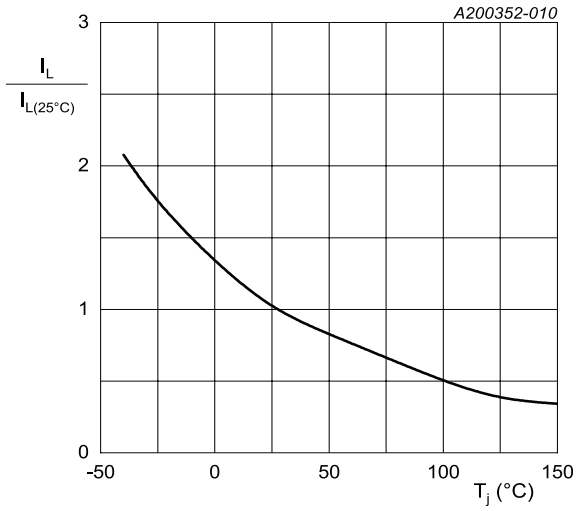


Fig. 8. Normalized latching current as a function of junction temperature

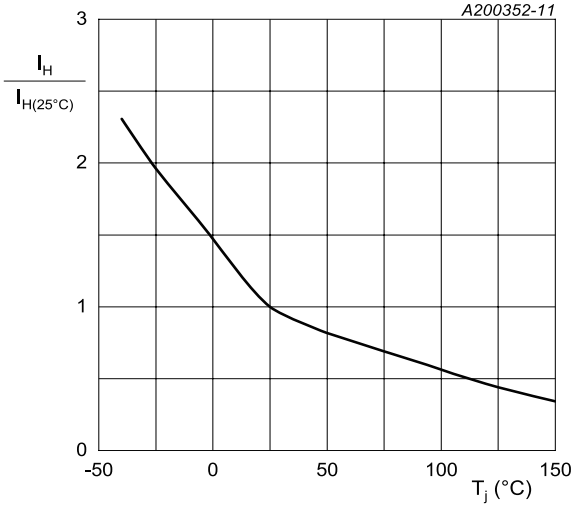
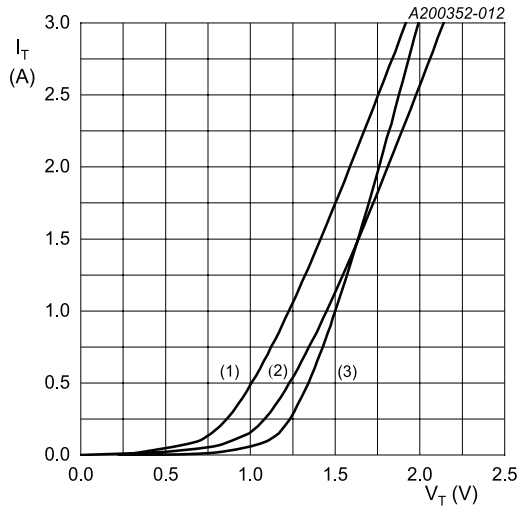


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.230 V; R_s = 0.2000 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

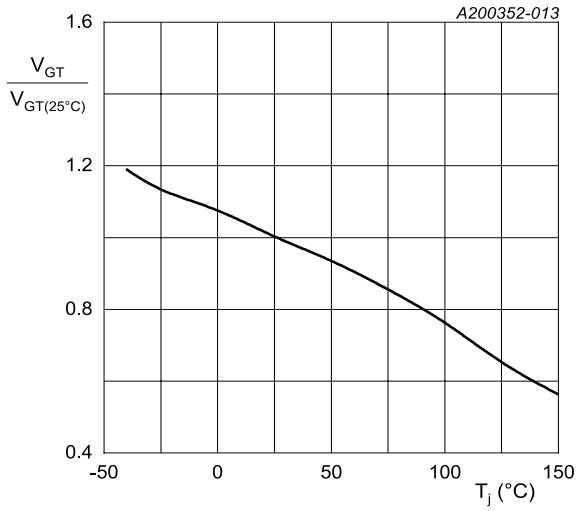
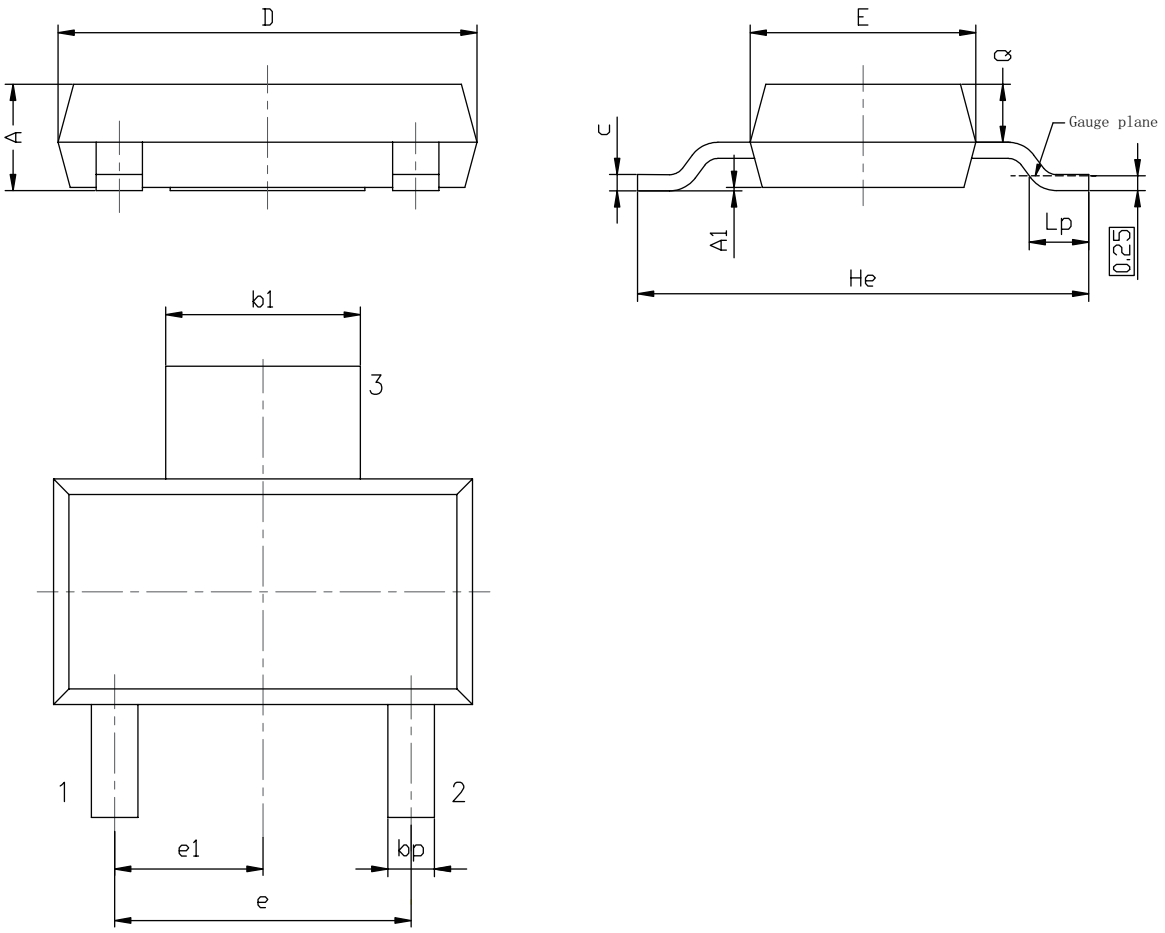


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline



Unit		A	A1	bp	b1	c	D	E	e	e1	He	Lp	Q
mm	Min	1.50	0.01	0.66	2.90	0.23	6.30	3.30	4.50	2.20	6.70	0.75	0.82
	Max	1.81	0.12	0.85	3.13	0.35	6.70	3.70	4.70	2.40	7.30	1.20	0.93

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

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